Title: METHOD FOR ERASING AN NROM CELL

## **REMARKS**

## Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohba et al.* (U.S. Patent No. 6,330,192 B1) in view of *Chung* (U.S. Pat. Pub. No. 2004/0185619 A1). Claims 1, 2, 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Wong* (U.S. Patent No. 6,160,739) in view of *Chung* (U.S. Pat. Pub. No. 2004/0185619 A1). Claims 1-4 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Haddad et al.* (U.S. Patent No. 6,172,909 B1) in view of *Chung* (U.S. Pat. Pub. No. 2004/0185619 A1). Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohba et al.* (U.S. Patent No. 6,330,192 B1) and *Chung* (U.S. Pat. Pub. No. 2004/0185619 A1) in view of *Mehrad* (U.S. Patent No. 5,576,922). Applicants respectfully traverse these rejections.

Ohba et al. disclose a method for erasing a non-volatile semiconductor memory device. After erasing has been completed, Ohba et al. perform an over-erase verify operation. If a cell is over-erased, a recovery operation is performed on a bit-by-bit basis. The recover operation is disclosed at column 12, lines 38 – 39 as applying voltages as shown in Fig. 61. These voltages are shown in Figure 61 as being a constant 7V on the gate and a constant 4V on the bit line of the selected bit. Ohba et al. therefore, neither teaches nor suggests Applicants' invention as claimed in the amended claims for performing an erase operation then performing a recovery operation that is comprised of applying a ramped voltage on the gate input.

Wong discloses a method for improving endurance of a non-volatile memory by selectively erasing only those cells requiring to be erased. The Examiner states that Wong has an erase operation and a recovery operation with the ramped gate input voltage of the present invention. However, Wong uses a ramped voltage as part of the erase operation to improve the endurance of a memory cell, not as a recovery operation from an erase operation. As stated in Wong at col. 13, lines 14 - 16, the control gate voltage is ramped from 0 volts down to the negative erase voltage of -8 to -10V.

Applicants' invention, as claimed in the amended claims, is to first performing an erase operation then performing a recovery operation that recovers over-erased cells from the erase operation. The ramped voltage is part of Applicants' recovery operation and not the erase operation as in *Wong*. This is not an obvious difference since Applicants are increasing the threshold voltage of an over-erased cell. *Wong* is decreasing the threshold voltage with the

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negatively ramped voltage in order to erase the cell. *Wong* thus neither teaches nor suggests Applicants' invention as currently claimed.

Haddad et al. disclose a ramped gate technique for soft programming a memory device. As stated in Haddad et al. at col. 8, lines 16-26, soft programming circuitry generates a ramped voltage for programming a flash memory cell. Applicants are claiming a method for erasing, not programming, a memory cell. Applicants' method, as claimed in the amended claims, first performs an erase operation then a recovery operation. This method for erasing is neither taught nor suggested by Haddad et al.

Mehrad discloses a method for extending the life of a floating gate memory cell using soft-programming. As seen in col. 6, lines 12 – 25 of Mehrad, the flash programming method is used to program all cells prior to erase. As discussed previously, Applicants' claimed invention is to a method for erasing a memory cell not programming or soft programming a memory cell. Applicants' claimed method first performs an erase operation then a recovery operation that is neither disclosed nor suggested by Mehrad. This is not an obvious difference since, as is well known in the art, the voltages and timing for programming a memory cell are different than those used for erasing a memory cell.

Chung discloses a non-volatile memory device using an oxide-nitride-oxide layer for charge storage. Chung neither teaches nor suggests Applicants' invention as currently claimed.

The already shown, the above-cited references neither teach nor suggest Applicants' invention as claimed in the amended claims. Additionally, even if it were obvious to combine either *Ohba et al.*, *Wong*, *Haddad et al.*, or *Mehrad* with *Chung*, and Applicants maintain that it is not, the combination still would not anticipate Applicants' claimed invention.

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## **CONCLUSION**

For the above-cited reasons, Applicants respectfully request that the Examiner withdraw the rejections and restriction requirement and allow claims 1-14 of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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